Institute / College Name :	Darbhanga College of Engineering		
Program Name	**B.Tech EEE**		
Course Code	100305		
Course Name	DIGITAL ELECTRONICS		
Lecture / Tutorial (per week):	3/1	**Course Credits**	5
Course Coordinator Name	Ms. Sweta Kumari		

1. Scope and Objectives of the Course

The course introduces Boolean algebra, Reduction techniques and demonstrates the design of logic gates. Knowledge of digital systems design based on combinational and sequential logic is also imparted. This course further teaches about PLD, Memories and Logic Families**.**

1. Understanding the different number systems used in computerized system and codes used to represent the digits and fundamental of arithmetic operation using each number system and codes.
2. Understanding the minimization of logic expression and designing combinational and sequential digital circuits.
3. Analyzing the operation and design constraints of CMOS and TTL circuit for logic fabrication.
4. Verifying and analyzing the practical digital circuits.
5. Enabling students to take up application specific sequential circuit to specify the finite state machine and designing the logic circuit.
6. Verify and analyze the input/output data of each logic gate and circuits such as adders, counters, coders, etc,
7. Analyze the basic operation of memory cell and its limitations in circuit designing.
8. Apply the digital circuit design concept in developing basic component of computer organization, projects or experiments.

2. Textbooks

TB1: Mano, Morris. "Digital logic." *Computer Design. Englewood Cliffs Prentice-Hall* (1979).
TB2: Kumar, A. Anand. *Fundamentals Of Digital Circuits 2Nd Ed*. PHI Learning Pvt. Ltd., 2009.
TB3: Digital systems - Principles and Applications by Tocci, Widmar and Jain, Pearson
TB4: Digital fundamentals by Floyd And Jain, Pearson

3. Reference Books

RB1: Fundamentals of VHDL design by Stephen Brown and Zovenkeo Vraseseic, TMH
RB2: Introduction To Logic Design With Cd Rom by Alan B Marcovity, TMH,
RB3. Fundamentals Of Digital Logic With Verilog Design by Stephen Brown, TMH
RB4. Modern digital electronics by R.P Jain, TMH

Other readings and relevant websites

S.No.	**Link of Journals, Magazines, websites and Research Papers**
1.	http://nptel.ac.in/courses/117106086/1
2.	http://nptel.ac.in/courses/117106114/
3.	http://www.engpaper.com/electronics.htm
4.	http://www.newelectronics.co.uk/digital-magazine/
5.	http://journalspub.com/journalspub/AllEditorsJournalwise.aspx?jid=25&jname=International+Journal+of+Digital+Electronics

6. Course Plan

Lecture Number	Date of Lecture	Topics	Web Links for video lectures	Text Book / Reference Book / Other reading material	Page numbers of Text Book(s)
1-4		**Digital Principle**		TB3, RB4	
		Analog vs Digital, Number system, Computer Codes, Digital Signals, Waveforms Positive and Negative logic, Logic Gate: basic, universal and others, Truth Table, Logic functions, IC Chips, Timing Diagram, and Electrical analogy.	https://www.youtube.com/watch?v=CeD2L6KbtVM		
Tutorial - 1					

5-9		**Boolean laws and theorems**		TB1,TB2	
		Logic functions, conversion of logic functions into truth table and vice versa. SOP and POS forms of representation, min terms and max terms, simplification of logic functions by theorems and Karnaugh's map, don't care conditions, design of special purpose computers and related practical problems.	https://www.youtube.com/watch?v=WfA4zlARZ7k		
Tutorial – 2, Assignment I					
9-15		**Analysis and synthesis of combinational logic circuits**		TB1, TB2, RB4	
		Adder and substructures (look ahead adders), Multiplexers, de multiplexers, Encoders, decoders, code convertors, magnitude comparators, parity generators and	https://www.youtube.com/watch?v=uv_RJ1Pv71s		
Tutorial - 3					
Mid-Semester Exam (Syllabus covered from 1-15 lectures)					
16-19		**Integrated circuit logic families**		TB3, RB1	
		RTL, DTL, TTL, CMOS, IIL/I2L (integrated injection logic & emitter coupled logic).	https://www.youtube.com/watch?v=iqENkJnJiwc		
Tutorial – 4, Assignment 2					
20-29		**Sequential circuit blocks and latches**		TB2, TB3, RB3	
		flip flops- race around condition, master slave and edge triggered, SR, JK, D & T Flip Flop, shift registers, counters- synchronous and asynchronous: design of ripple counter.	https://www.youtube.com/watch?v=ibQBb5yEDlQ		
Tutorial - 5					
30-31		**Timing circuit**		TB1, RB2	
		multi vibrators, mono stable and astable timer: LM555	https://www.youtube.com/watch?v=tpVUl_y0EyQ		
Tutorial 6					
32-33		**Use of building blocks**		TB1, RB4	
		designing larger systems such as digital to analog converters(DAC) weighted resistors and r-2r , analog to digital(ADC)- comparator, counter and succession.	https://www.youtube.com/watch?v=Y2OPnrgb0pY		
Tutorial - 7					
34-35		**Memories**		TB1, TB2, RB4	
		static and dynamic RAMs, ROM, EPROM, and EEPROM.	https://www.youtube.com/watch?v=GnOTczdBWh8		
Tutorial – 8, Assignment 3					

1. **Evaluation Scheme:**

Component 1	Mid Semester Exam	20
Component 2	Assignment Evaluation	10
Component 3**	End Term Examination**	70
	Total	**100**

****** The End Term Comprehensive examination will be held at the end of semester. The mandatory requirement of 75% attendance in all theory classes is to be met for being eligible to appear in this component.

SYLLABUS

Topics	No of lectures	Weightage
Digital Principle: Analog vs Digital, Number system, Computer Codes, Digital Signals, Waveforms Positive and Negative logic, Logic Gate: basic, universal and others, Truth Table, Logic functions, IC Chips, Timing Diagram, and Electrical analogy.	4	11%
Boolean laws and theorems: Logic functions, conversion of logic functions into truth table and vice versa. SOP and POS forms of representation, min terms and max terms, simplification of logic functions by theorems and Karnaugh's map, don't care conditions, design of special purpose computers and related practical problems.	5	14%
Analysis and synthesis of combinational logic circuits : Adder and substructures (look ahead adders), Multiplexers, de multiplexers, Encoders, decoders, code convertors, magnitude comparators, parity generators and Checkers.	6	16%
Integrated circuit logic families: RTL, DTL, TTL, CMOS, IIL/I2L (integrated injection logic & emitter coupled logic).	4	12%
Sequential circuit blocks and latches, flip flops- race around condition, master slave and edge triggered, SR, JK, D & T Flip Flop, shift registers, counters- synchronous and asynchronous: design of ripple counter.	10	29%
Timing circuit: multi vibrators, mono stable and astable timer: LM555.	2	6%
Use of building blocks in designing larger systems such as digital to analog converters(DAC) weighted resistors and r-2r , analog to digital(ADC)-comparator, counter and succession.	2	6%
Memories: static and dynamic RAMs, ROM, EPROM, and EEPROM.	2	6%

This Document is approved by:

Designation	Name	Signature
Course Coordinator	Ms. Sweta Kumari	
H.O.D	Mr. Prabhat Kumar	
Principal	Dr. Achintya	
Date	24-02-2021	

Evaluation and Examination Blue Print:
Internal assessment is done through quiz tests, presentations, assignments and project work.

The components of evaluations along with their weightage followed by the University is given below

Sessional Test	20%
Assignments/Quiz Tests/Seminars	10%
End term examination	70%

Vision of EEE: - To bring forth engineers with an emphasis on higher studies and a fervour to serve national and multinational organisations and, the society.

Mission of EEE: -

M1: - To provide domain knowledge with advanced pedagogical tools and applications.
M2: - To acquaint graduates to the latest technology and research through collaboration with industry and research institutes.
M3: - To instil skills related to professional growth and development.
M4: - To inculcate ethical valued in graduates through various social-cultural activities.

PEO of EEE

PEO 01 – The graduate will be able to apply the Electrical and Electrical Engineering concepts to excel in higher education and research and development.
PEO 02 – The graduate will be able to demonstrate the knowledge and skills to solve real life engineering problems and design electrical systems that are technically sound, economical and socially acceptable.
PEO 03 – The graduates will be able to showcase professional skills encapsulating team spirit, societal and ethical values.

PSO of EEE

PSO 01 Students will be able to identify, formulate and solve problems using various software and other tools in the areas of Automation, Control Systems, Power Engineering and PCB designing.
PSO 02 Students will be able to provide sustainable solutions to growing energy demands.

Scope and Objectives of the Course

The course introduces Boolean algebra, Reduction techniques and demonstrates the design of logic gates. Knowledge of digital systems design based on combinational and sequential logic is also imparted. This course further teaches about PLD, Memories and Logic Families**.**

After the completion of this course the students will be able to:

CO 1: Enumerate basic logic gates, its symbols, Truth tables, Boolean equations, & working principle of the logic circuits.
CO 2: Application of logic gates to construct integrated circuits like TTL, CMOS; using one of several different designs, usually with compatible logic levels and power supply characteristics.
CO 3: Design both combinational and sequential networks such as multiplexers, adders, counters, coders, etc,
CO 4: Choose how to interface digital circuits with analog components (ADC, DAC, etc.).

DARBHANGA COLLEGE OF ENGINEERING,

DARBHANGA w.e.f. – 29-01-18

EEE

Day	1 (10am-10.50am)	2 (10.50am-11.40am)	3(11.40am-12.30pm)	4(12.30pm-1.20pm)	Lunch (1.20pm – 1.50pm)	5(1.50pm – 2.40pm)	6(2.40pm-3.30pm)	7(3.30pm-4.20pm)
Monday							Digital Electronics	
Tuesday								
Wednesday								
Thursday				Digital Electronics				
Friday		Digital Electronics						
Saturday						Digital Electronics		

Mapping of CO's with PO's

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	2	1	-	-	1	-	-	2	-	-	-	-	2	-
CO 2	1	2	-	-	1	-	-	-	-	-	-	1	2	2
CO 3	3	3	2	-	2	-	-	-	-	-	-	2	3	2
CO 4	2	1	1	-	-	2	1	-	1	1	-	1	1	1

DARBHANGA COLLEGE OF ENGINEERING

Department of Electrical and Electronics Engineering

Digital Electronics (041402)

Assignment II

1. What is Combinational Circuits.
2. Use a multiplexer to implement the logic function F =A ⊕ B ⊕ C.
3. Design the following combinational circuits :
   i. Full adder
   ii. Full subtractor

DARBHANGA COLLEGE OF ENGINEERING

Department of Electrical and Electronics Engineering

Digital Electronics (041402)

Assignment I

4. Multiple choice questions :

   i. The given hex number (1E.53)16 is equivalent to
      a) (35.68)8
      b) (35.24)8
      c) (34.34)8
      d) (35.59)8
   ii. The octal number (651.124)8 is equivalent to
      a) (1A9.260)16
      b) (1B0.160)16

c) (1A8.023)16

d) (1B0.289)16

iii. Convert hexadecimal to decimal: (1E2H) = ?

a) 480

b) 483

c) 482

d) 484

iv. (170)10 is equivalent to

a) (FD)16

b) (DF)16

c) (AA)16

d) (AF)16

v. Convert in to decimal: (214)8 = ?

a) (140)10

b) (141)10

c) (142)10

d) (130)10

vi. Convert (0.345)10 in to an octal number.

a) (0.1605)8

b) (0.2605)8

c) (0.1945)8

d) (0.2404)8

vii. Convert from binary to decimal: (01011.1011)2 = ?

a) (11.6875)10

b) (11.5874)10

c) (10.9876)10

d) (10.7893)10

viii. Octal to binary conversion: (24)8 = ?

a) (111101)2

b) (010100)2

c) (111100)2

d) (101010)2

ix. Convert binary to octal: (110110001010)2 = ?

a) (5512)8

b) (6612)8

c) (4532)8

d) (6745)8

5. i) Reduce the expression Σ m(0,2,3,4,5,6) using mapping and implement it in AOI logic as well as in NAND logic.

6. ii) Reduce the expression Π M(0,1,2,3,4,7) using mapping and implement it in AOI logic as well as in NAND logic.

DARBHANGA COLLEGE OF ENGINEERING

Department of Electrical and Electronics Engineering

Digital Electronics (041402)

Assignment III

1. Design and implement a mod-10 asynchronous counter using T FFs.
2. What is the difference between the counting sequence of an up-counter and a down counter?
3. Describe how an asynchronous down-counter circuit differs from an up-counter circuit.
4. What is ROM? Explain types of ROM.

Darbhanga College of Engineering

EEE Department

Mid. Sem Exam

Digital Electronics

Time: 2 Hours ***Max. Marks: 20***

Note: ***Attempt all four questions.***

1. Determine the base/ code as desired below: [5]

   i) $(444.456)_{10} = (\ )_8$ ii) $(2D5)_H = (\ )_2$

   iii) $[10101101]_2 = [\ ]_G$ iv) $[1010111]_G = [\ ]_2$

   OR

   Determine the Canonical ***SOP*** *and* Canonical ***POS*** function $Y = A + BC$ and also determine product of maxterm of $F = XY + XZ$

[5]

2. With the help of neat diagram explain the working of a two-input TTL NAND gate.
[5]

3. Simplify and apply the following using minimum Logic Gates
[5]

$$Y = \overline{\overline{A\bar{B}+ABC+A\,(B+A\bar{B})}}$$

OR

Design and implement the BCD to Excess-3code converter circuit using minimum number of Logic Gates.
[5]

4. (a) What is the function of ADCs and DACs?
[2]

(b) Briefly explain the R-2R ladder DAC.
[3]

Syllabus

Digital Electronics

Course Code- 041402

L-T-P : 3-1-2 **Credit : 5**

1. Digital Principle : Analog vs Digital, Number system, Computer Codes, Digital Signals, Waveforms Positive and Negative logic, Logic Gate : basic, universal and others, Truth Table, Logic functions, IC Chips, Timing Diagram, Electrical analogy.

2. Boolean laws and theorems : Logic functions, conversion of logic functions into truth table and vice versa. SOP and POS forms of representation, min terms and max terms, simplification of logic functions by theorems and Karnaugh's map, don't care conditions, design of special purpose computers and related practical problems.

3. Analysis and synthesis of combinational logic circuits : Adder and substructures (look ahead adders), Multiplexers, de multiplexers, Encoders, decoders, code convertors, magnitude comparators, parity generators and checkers.

4. Integrated circuit logic families : RTL, DTL, TTL, CMOS, IIL/I2L (integrated injection logic & emitter coupled logic).

5. Sequential circuit blocks and latches, flip flops- race around condition, master slave and edge triggered, SR, JK, D & T Flip Flop, shift registers, counters- synchronous and asynchronous: design of ripple counter.

6. Timing circuit : multi vibrators, mono stable and astable timer: LM555.

7. Use of building blocks in designing larger systems such as digital to analog converters(DAC) weighted resistors and r-2r , analog to digital(ADC)- comparator, counter and succession.

8. Memories : static and dynamic RAMs, ROM, EPROM, EEPROM.

GATE Syllabus :
Combinational and Sequential logic circuits, Multiplexer, Demultiplexer, Schmitt trigger, Sample and hold circuits, A/D and D/A converters.

YEAR -2014

Code : 041402

B.Tech. 4th Semester Exam., 2014

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

(iv) Question No. 1 is compulsory.

1. Choose the correct option from the following (any *seven*) : 2×7=14

(a) A quantity having continuous wave is
- (i) a digital quantity
- (ii) an analog quantity
- (iii) a binary quantity
- (iv) a natural quantity

(b) The sum of 11010+01111 equals
- (i) 101001
- (ii) 101010
- (iii) 110101
- (iv) 101000

(c) The output of a gate is low if and only if its input are HIGH. It is true for
- (i) AND
- (ii) XNOR
- (iii) NOR
- (iv) NAND

(d) An example of a standard SOP expression is
- (i) $\overline{A}\overline{B}+A\overline{B}C+A\overline{B}\overline{D}$
- (ii) $A\overline{B}C+ACD$
- (iii) $A\overline{B}+\overline{A}B+AB$
- (iv) $AB\overline{C}D+\overline{A}B+\overline{A}$

(e) To implement the expression of $\overline{A}BCD+A\overline{B}CD+AB\overline{C}\overline{D}$, it takes one OR gate and
- (i) one AND gate
- (ii) three AND gates
- (iii) three AND gates and four inverters
- (iv) three AND gates and three inverters

(f) The invalid state of an *S-R* latch occurs when
- (i) $S=1, R=0$
- (ii) $S=0, R=1$
- (iii) $S=1, R=1$
- (iv) $S=0, R=0$

(g) The device used to convert a binary number to a 7-segment display format is

(i) multiplexer

(ii) encoder

(iii) decoder

(iv) register

(h) An asynchronous counter differs from a synchronous counter in

(i) the number of states in its sequence

(ii) the method of clocking

(iii) the type of flip-flop used

(iv) the value of the modulus

(i) A stage in a shift register consists of

(i) a latch

(ii) a flip-flop

(iii) a byte of storage

(iv) four bits of storage

(j) A 32-bit data word consists of

(i) 2 bytes

(ii) 4 nibbles

(iii) 4 bytes

(iv) 3 bits and 1 nibble

(Turn Over)

2. (a) Make a K-map for the function

$$F = A\bar{B} + AC + A\bar{D} + AB + ABC$$ 5

(b) Express F, in standard SOP and POS form. 5

(c) Minimize F and realize the minimal expression using NOR gate only. 4

3. (a) Prove the following algebraically : 2½+2½=5

(i) $(A+B)(A+\bar{B}) = A \oplus B$

(ii) $(A+B)(A+\bar{B})(\bar{A}+B) = AB$

(b) Convert decimal number 75 into Grey code. 4

(c) Verify a two-level AND-OR gate is equivalent to NAND-NAND. 5

4. (a) Draw a circuit diagram of an RTLEX-OR gate. Explain its operation. 7

(b) Draw a circuit diagram of DTL gate and explain it. What are fan-in and fan-out? How will you increase the fan-out of the gate? 7

5. (a) Design a full adder using only NAND gate. 7

(b) Design a 8 to 1 line multiplexer using 4 to 1 line multiplexer. 7

6. (a) Differentiate between synchronous and asynchronous counter. 7

(b) Design a 4-bit synchronous up counter. 7

7. (a) Explain the following flip-flops with their diagrams and truth tables : 7

(i) SR F/F

(ii) J-K F/F

(iii) D F/F

(iv) T F/F

(b) Design D F/F from J-K F/F. 7

8. (a) Explain the working principle of a successive approximation ADC with the help of circuit diagram. 7

(b) Find the output voltage from a 5-bit ladder D/A converter which has a digital input of 11010. Assume 0 = 0 V and 1 = +10 V. 7

9. Write short notes on any *two* of the following : 7×2=14

(a) Data transfer in a shift register

(b) ROM

(c) Astable multivibrator using 555

(d) Digital comparator

YEAR -2015

Code : 041402

B.Tech 4th Semester Exam., 2015

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Choose the correct option from any *seven* of the following : 2×7=14

(a) Digital circuits mostly use

(i) diodes

(ii) bipolar transistors

(iii) diodes and bipolar transistors

(iv) bipolar transistors and FET

(b) Which of the following binary numbers is equivalent to decimal number 10?

(i) 1000

(ii) 1100

(iii) 1010

(iv) 1001

(c) In a three-input NOR gate, the number of states in which output is one, equals

(i) 1

(ii) 2

(iii) 3

(iv) 4

(d) In which function each term is known as max term?

(i) SOP

(ii) POS

(iii) Hybrid

(iv) Both (i) and (ii)

(e) Digital technologies being used now-a-days are

(i) DTL and EMOS

(ii) TTL, ECL, CMOS and RTL

(iii) TTL, ECL and CMOS

(iv) TTL, ECL, CMOS and DTL

(f) A Karnaugh map with four variables has

(i) 2 cells

(ii) 4 cells

(iii) 8 cells

(iv) 16 cells

(g) A three-bit binary adder should use

(i) 3 full adders

(ii) 2 full adders and one half adder

(iii) 1 full adder and 2 half adders

(iv) 3 half adders

(h) Which device changes parallel data to serial data?

(i) Decoder

(ii) Multiplexer

(iii) Demultiplexer

(iv) Flip-flop

(i) A mod 4 counter will count

(i) from 0 to 4

(ii) from 0 to 3

(iii) from any number n to $n+4$

(iv) None of the above

(j) The access time of ROM using bipolar transistor is about

(i) 1 sec

(ii) 1 milisec

(iii) 1 microsec

(iv) 1 nanosec

2. (a) Convert the following decimal number into binary numbers :

(i) $(39 \cdot 12)_{10}$

(ii) $(675 \cdot 634)_{10}$

(b) Convert the following into binary numbers :

(i) $(278)_8$

(ii) $(E7\ F6)_{16}$

(c) Write truth table for 3-input XOR gate and realize it by using NOR gate.

(d) Convert decimal number 35 into gray code. 4+3+4+3=14

3. (a) Simplify the function and draw a circuit to realize the simplified function

$$Y = [A\bar{B}\,(C + BD) + \bar{A}\,\bar{B}]C$$

(b) $Y = \Pi\, M(0, 1, 3, 5, 6, 7, 10, 14, 15)$
Draw the logic circuit for the simplified function. 6+8=14

4. (a) Explain the operation of TTL NAND gate with totem pole output.

(b) What is the difference between current sourcing and current sinking? 8+6=14

5. (a) What is the difference between decoder and encoder? Draw the logic circuit of decimal to BCD encoder and explain its working.

(b) What is demultiplexer? Draw its block diagram and explain its working. 7+7=14

6. (a) Differentiate between combinational circuit and sequential circuit.

(b) Explain the working of S-R flip-flop with the help of a neat diagram. 6+8=14

7. (a) Draw the circuit of a 4-bit ripple counter. Explain its working. Draw its timing diagram.

(b) Draw the circuit of a serial-in, serial-out shift resistor and explain its working. 7+7=14

8. (a) Draw the circuit of a binary ladder network A/D converter and explain its working.

(b) Draw a circuit of astable multivibrator using timer 555 and explain its working. 7+7=14

9. Write short notes on any two of the following : 7×2=14

(a) EPROM

(b) ROM

(c) Full subtractor and half subtractor

(d) Magnitude comparators

★★★

YEAR -2016

9. Write notes on the following : 5+5+4=14

(a) Monostable multivibrator using 555 timer

(b) RAMs

(c) ECL

* * *

B.Tech 4th Semester Exam., 2016

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Fill in the blanks (any *seven*) : 2×7=14

(a) The number of rows in truth table of 04 variables is ___.

(b) The number of 3-input NAND gates in a 14-pin IC is ___.

(c) The number of characters represented by ASCII code is ___.

(d) The distance between the code words 10010 and 10101 is ___.

(e) Power dissipation is negligibly small in ___ devices.

(f) ___ is the fastest logic family.

(g) The figure of merit of a digital IC is given by ___.

(h) ___ code is used for labelling the cells of K-map.

(i) Subtractors are designed using ___ ICs.

(j) Registers and counters can be designed using ___.

2. (a) Determine the decimal numbers represented by the binary number

$$(101101.1010)_2$$

(b) Convert $(10.625)_{10}$ in the binary form.

(c) Subtract (7 – 5) using 2's complement representation of negative number. 5+5+4=14

3. Design 4-bit Binary-to-Gray code converter circuits. 14

4. (a) Implement the following multi-output combinational logic circuit using a 4-to-16 line decoder :

$F_1 = \Sigma m(1, 2, 4, 7, 8, 11, 12, 13)$

$F_2 = \Sigma m(2, 3, 9, 11)$

$F_3 = \Sigma m(10, 12, 13, 14)$

$F_4 = \Sigma m(2, 4, 8)$

(b) Realize $f_1 = \Sigma m(0, 3, 5, 6, 9, 10, 12, 15)$ using 8 : 1 multiplexers. 7+7=14

5. (a) Draw master-slave J-K flip-flop using NAND gates.

(b) Explain a 4-bit bidirectional shift register with neat circuit diagram. 7+7=14

6. (a) Design a 3-bit binary UP/DOWN counter with a direction control M. Use J-K flip-flops.

(b) Draw modulo-125 ripple counter. 10+4=14

7. (a) Draw CMOS NAND gates and NOR gates.

(b) Draw NOT gate, OR gate and AND gate using RTL.

(c) Draw TTL with totem pole output and explain its operation. 4+5+5=14

8. (a) Define the following characteristics of a D/A converter :

(i) Resolution

(ii) Linearity

(iii) Accuracy

(iv) Settling time

(v) Temperature sensitivity

(b) Draw and explain 3-bit parallel comparator (flash) A/D converter. 7-7=14

YEAR -2017

Code : 041402

B.Tech 4th Semester Examination, 2017

Digital Electronics

Time : 3 hours *Full Marks : 70*

Instructions :

*(i) There are **Nine** Questions in this Paper.*

*(ii) Attempt **Five** questions in all.*

*(iii) **Question No. 1 is Compulsory.***

(iv) The marks are indicated in the right-hand margin.

1. Fill in the blanks. 7×2

(a) The MSB of a signal-binary number indicates its_____.

(b) The principle cause of propagation delay in a p-n junction is removal of_____ charge carriers.

(c) Fan-in signifies_____ of a gate.

(d) The temperature range for 74-series ICs is _____.

(e) AND-OR realization is equivalent to_____ realization.

(f) A_____ is a logic circuit that accepts one data input and distributes it over several outputs.

(g) sub tractors are designed using_____ICs.

(h) Register and counters can be designed using_____.

(i) Ripple counter is_____ sequential circuits.

(j) The linearity of a D/A converter is specified as ____ LSB.

2. (a) Draw EX-OR gates using only 4-NAND gates only.

(b) Draw NAND gates using Transistors and Resisters.

(c) Convert $(11111)_2$ into gay code. 14

3. (a) Find the range of V_{BB} for the transistor shown in figure (3.1) or

(i) in the cut-off region

(ii) in the active region

(iii) in the saturation region

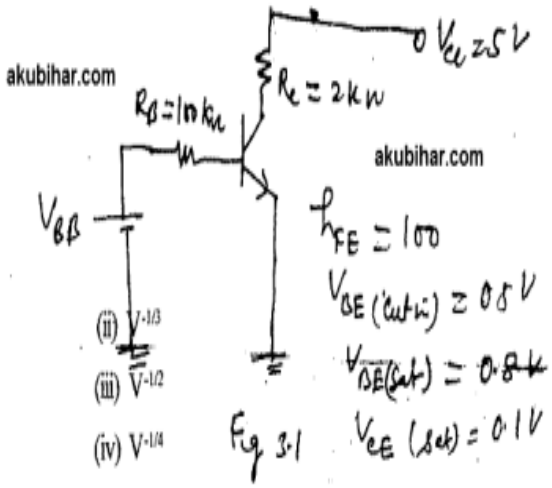

Fig 3.1

(b) Analyse TTL gate with totem pole output driver. 6+8

4. (a) Minimise in POS form

$$f(A,B,C,D) = \prod M(4, 6, 10, 12, 13, 15)$$

(b) Minimise $f(A,B,C,D) = A\bar{B}\bar{C}D + \bar{A}BCD + \bar{A}\,\bar{B}\,\bar{C} + \bar{A}\,\bar{B}\,\bar{D} + A\,\bar{C} + A\,\bar{B}\,C + \bar{B}$ 14

5. (a) Design 16 : 1 multiplexer using 8:1 MUX.

(b) Design 3-bit Gray-to-Binary Converter. 6+8

6. (a) Explain Race-Around condition.

(b) Draw J-K flip-flop and explain its operation.

(c) Draw D-Flip flop and T-flip flop wing J-K FF.

 4+6+4

7. (a) Design modulo-10 synchronous counter using J-K flip flop.

(b) Explain lock-out condition in counter.

(c) Draw 4-bit left to Right shaft register and explain its operation. 7+3+4

8. (a) Draw 3-bit successive type A/D converter and explain its operator.

(b) Explain basic blocks of 555-timer. 8+6

9. Write notes on following-

(a) RAMs.

(b) Non-saturated logic families. 7+ 7

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DARBHANGA COLLEGE OF ENGINEERING, DARBHANGA

3rd Sem. Branch:- EEE Batch- (2019-22)
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68	ADITYA KUMAR	20LE-EE04	20110111906
69	SANTOSH KUMAR	20LE-EE10	20110111907
70	ADITYA KUMAR	20LE-EE13	20110111908
71	RAKESH KUMAR JHA	20LE-EE12	20110111909
72	ANJALI KUMARI	20LE-EE03	20110111910
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